CLAIMS

1. (Previously Presented) A computer-implemented method for hierarchical very large scale integration design comprising:

representing a structure of the hierarchical very large scale integrated design as a graph comprising design objects;

specifying a transformation behavior applied to the design objects;

processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design; and

outputting a transformed hierarchical very large scale integrated design.

2. (Previously Presented) The computer-implemented method of claim 1, wherein the processing further comprises searching for an isomorphic structure.

3. (Previously Presented) The computer-implemented method of claim 1, wherein the graph describes a plurality of scopes.

4. (Previously Presented) The computer-implemented method of claim 1, wherein the graph is based on a pointset interaction between structures of the hierarchical very large scale integration design.

5. (Previously Presented) The computer-implemented method of claim 1, wherein the graph is based on symmetry groups between structures of the hierarchical very large scale integration design, wherein the graph represents a circuit substructure.

6. (Previously Presented) The computer-implemented method of claim 1, wherein an attribute is attached to a design object, the attribute having a user-defined mapping between an attribute transformation and a design object transformation.

7. (Previously Presented) The computer-implemented method of claim 1, wherein processing, top-down, comprising transferring information from a child graph to a parent graph, wherein a node in the parent graph represent an instance of the child graph.

8. (Previously Presented) The computer-implemented method of claim 1, wherein processing, top-down, the graph comprises resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph.

9. (Previously Presented) The computer-implemented method of claim 8, wherein each cell is represented by a plurality of connected least enclosing orthogonal pointsets.

10. (Previously Presented) The computer-implemented method of claim 9, further comprising:

determining an interaction between the least enclosing orthogonal pointsets; and

determining a decomposition of the cell according to the interaction.

11. (Previously Presented) The computer-implemented method of claim 10, wherein processing, top-down, further comprises cloning by expression using a result of the decomposition to produce a cell definition.

12. (Previously Presented) The computer-implemented method of claim 1, wherein representing the structure of the hierarchical very large scale integration design as the graph comprising design objects further comprises determining a plurality of scopes, wherein each scope comprises an internal node and a leaf node.

13-15. (Cancelled)

16. (Previously Presented) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for hierarchical very large scale integration design, the method steps comprising:

representing a structure of the hierarchical very large scale integrated design as a graph comprising design objects;

specifying a transformation behavior applied to the design objects;

processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design; and

outputting a transformed hierarchical very large scale integrated design.

17. (Original) The method of claim 16, wherein the processing further comprises searching for an isomorphic structure.

18. (Original) The method of claim 16, wherein the graph describes a plurality of scopes.

19. (Original) The method of claim 16, wherein the graph is based on a pointset interaction between structures of the hierarchical very large scale integration design.

20. (Original) The method of claim 16, wherein the graph is based on symmetry groups between structures of the hierarchical very large scale integration design, wherein the graph represents a circuit substructure.

21. (Original) The method of claim 16, wherein an attribute is attached to a design object, the attribute having a user-defined mapping between an attribute transformation and a design object transformation.

22. (Original) The method of claim 16, wherein processing, top-down, comprising transferring information from a child graph to a parent graph, wherein a node in the parent graph represent an instance of the child graph.

23. (Original) The method of claim 16, wherein processing, top-down, the graph comprises resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph.

24. (Original) The method of claim 23, wherein each cell is represented by a plurality of connected least enclosing orthogonal pointsets.

25. (Original) The method of claim 24, further comprising:

determining an interaction between the least enclosing orthogonal pointsets; and

determining a decomposition of the cell according to the interaction.

26. (Original) The method of claim 25, wherein processing, top-down, further comprises cloning by expression using a result of the decomposition to produce a cell definition.

27. (Original) The method of claim 16, wherein representing the structure of the hierarchical very large scale integration design as the graph comprising design objects further comprises determining a plurality of scopes, wherein each scope comprises an internal node and a leaf node.

28. (Previously Presented) A computer-implemented method for hierarchical very large scale integration design comprising:

representing a structure of the hierarchical very large scale integrated design as a graph comprising design objects;

specifying a transformation behavior applied to the design objects;

processing the graph top-down beginning with a root cell of the graph to perform the transformation behavior on the hierarchical very large scale integrated design, wherein the transformation behavior resolves a boundary condition of the hierarchical very large scale integrated design by performing a move operation, a split operation or a merge operation to adjust the structure of the hierarchical very large scale integrated design; and

outputting a transformed hierarchical very large scale integrated design.

29. (Previously Presented) The computer-implemented method of claim 28, wherein each cell is represented by a plurality of connected least enclosing orthogonal pointsets, the computer-implemented method further comprising:

determining an interaction between the least enclosing orthogonal pointsets; and

determining a decomposition of the cell according to the interaction.

30. (Previously Presented) The computer-implemented method of claim 29, wherein processing, top-down, further comprises cloning by expression using a result of the decomposition to produce a cell definition.